-A- Motivation & Objectives

The number of working groups addressing the debug standards largely increased recently (2 in 2002, 4 in 2004, 8 in 2006, 10-11 in 2007?). Potentially, there is some overlap in these standardization efforts.

We need to ensure that we address the right problems with adequate solutions in terms of practical and adopted standards. To do so first we need to have a clear picture what are the key advanced features the standardization should address: SW interface and APIs?, performance issues?, next generation JTAG?

There is a need to understand various standardization efforts and activities in the area of SoCs integration debug: their content, scope, status and roadmaps.

The workshop will present the landscape of the standardization activities, with their objectives, motivation and technical advancement. It will also give the possibility to the SoC developers to express their needs in terms of methods, required standards and tool support.

The outcome will be to have a better understanding of the industry needs, emerging solutions and missing parts in the SoC debug area.

-B- Structure

Session 1: Introduction
In the first session an overview and a “topology map” of the existing standardization activities will be presented, as well as their relations to industry initiatives and de facto standards.

Session 2: Industry Needs and Requirements
This session will give the opportunity to industry users to express their requirements in area of debugging on methods, standards, missing capabilities, features.
They may also talk about their experiments with emerging standards, or bring the motivation for standardization activities to be set-up (e.g. within SPIRIT or OCP-IP).
Invited are: STMicroelectronics, Infineon, NXP, Thomson, Nokia, ARM.

Panel in session 2: What is the most important issue to be addressed by standardization? Do we have converging industry requirements?

Session 3: Standardization Activities
The session 2 will provide an overview of the existing or emerging standardization work. The identified activities are:
- SPIRIT Debug WG
- IEEE P1687 IJTAG
- IEEE 1149.7 CJTAG
- Nexus 5001
- MIPI Test & Debug WG
- OCP-IP (emerging) Debug WG
- Multicore Association Debug WG
- SPRINT Project Debug WG
- GreenSocs

Panel in Session 3: Overlap or complementarities between standardization activities?

Session 4: Industrial Debug Solutions
- Cadence’s Entreprise System Level Verification
- ARM RealViiew Debug APIs
- ARM CoreSight SoC Debug Architecture
- Lauterbach
- Eclipse (WindRiver)
- MCDS – Multi-Core Debug Solution
- Mentor Graphics SW Debug Solutions
- Green Hills Software
- CoWare Debug
- Lokesh Gupta from NXP: View on Multi-core Debug Standardization

At NXP, we develop complex SoCs and there is an ever increasing need for a robust Multi-core debug environment. The Multi-core debug environment should bring together all connected debuggers and the target design into a unified debug view of the whole system. It should work with target designs seamlessly throughout the entire design and development lifecycle from models of the SoC to FPGA based verification setups as well as with real silicon. To achieve these goals, we foresee the need for standardization both from the tools side as well as from the IP vendors side. In this presentation, we would highlight these two areas of standardization, and participation of NXP in the development of these standards.

- Albrecht MAYER from INFINEON

- Industry Needs & Requirements

**Debugging Needs from Zero Tool Cost Low End to Zero Defect Automotive**

Traditional software and system debugging based on breakpoints, single stepping and instrumentation definitely comes to its limit for multi-core SoCs working in real time environments. In the automotive industry, where absolute reliability is key for market success, high end debug solutions have been constantly used. The challenge is to provide powerful debug features in particular tracing with a minimum cost adder for the SoC mass production. On the other side of the spectrum are 8 or 16-bit microcontroller where some customers expect no or very little tool cost. This presentation will cover the different requirements, show existing solutions and the remaining gaps.

- Standardization

**SPRINT Debug WG**

SPRINT is a European funding project to create an Open SoC Design Platform for Reuse and Integration of IPs [www.ecsi-association.org/sprint](http://www.ecsi-association.org/sprint). In work package 4 (WP4) the target is to create standard interfaces (APIs) between on the one hand debug and profiling tools and on the other hand a system modelled at a given abstraction level or the real silicon with physical tool access hardware. WP4 members are all major European semiconductor vendors (Infineon, NXP, ST) major tool providers (ARM, Lauterbach) and the TIMA research lab. All involved companies see a strong need for a standard here to create a market for IP simulation models with debug features and to reduce tool targeting cost for SoC models and silicon.

- Industrial Debug Solutions

**Multi-Core Debug Solution MCDS**

For multi-core SoCs Infineon decided in cooperation with key customers to create an on-chip Multi-Core Debug Solution (MCDS) which features trace, triggers and performance monitoring. The prospect for the future shows that on-chip trace is the only long term sustainable real time debug approach. Devices with MCDS and associated tooling are available in the market and are used with very positive feedback from automotive customers. Infineon decided to partner with IPextreme to make the MCDS technology available to the industry to create an attractive market for associated tooling which benefits tool vendors (market size) and users (tool cost and quality).

- Neal STOLLON from MIPS Technologies

**Session 1 On Chip Debug - What Do We Have, What Do We Need**

This is introductory summary to diverse issues on the IP, tools, and infrastructure for on-chip debug of both HW and SW. There are several types of available solutions, but there is work needed for an integrated environment, which is what designers are looking for. We look at some items to consider during the rest of the workshop.
Session 3 Nexus 5001

Nexus Abstract: Nexus Forum is sponsoring organization for IEEE 5001 On Chip Debug standard. Nexus solutions have been implemented in many products, and has become a defacto requirement in parts of the automotive industry. We overview Nexus technology and discuss some of the experience of being a industry organization in this area.

Session 3 IJTAG + MCA + OCP-IP

I would like OCP-IP presentation listed separately (taking 15 minutes from the time slot) since this may be given by Bob Uvacek from Pixelworks, who I believe is attending the workshop.

OCP-IP abstract: OCP-IP has a Debug Working Group that has defined a Debug Interface Socket architecture for SoC debug. We discuss relevant areas of the OCP-IP background and specific types of debug requirements and interfaces being proposed.

IJTAG + MCA abstract: IJTAG is addressing next generation interfaces that integrate test and debug requirements that exceed 1149.1 JTAG. The MultiCore Association (MCA) is looking at the specific requirements related to debug of multicore systems and compatibility with MCA Communications API development.

Session 4 FS2/MIPS Debug products presentation

FS2/MIPS Abstract: FS2 has been involved in developing Design for Debug solutions since 1998 and has been innovator in both processor and system level integrated On Chip Instrumentation solutions. We discuss our solutions and technology developed to address specific IP and tools for on-chip debug.