0830 – 0840 **Introduction**
⇓ P Coussy, University of South Brittany, FR and A Morawiec, ECSI, FR

**SESSION 1: EDA TOOL PRESENTATIONS**

0845 - 0900 **Catapult Synthesis: a Proven Approach for the Creation of Complex Hardware Designs**
⇓ Bollaert, Mentor Graphics FR

0905 – 0920 **How to Make Algorithmic Synthesis as Ubiquitous as Logic Synthesis**
⇓ V Kathail, Synfora, US

0925 – 0940 **Cynthesizer: the Forte SystemC synthesis tool**
⇓ M Meredith, Forte Design Systems, US

0945 – 1000 **New Opportunities for High-Level Synthesis**
⇓ J Cong, UCLA/AutoESL, US

1000 – 1015 **BREAK**

**SESSION 2: RESEARCH DIRECTIONS**

1020 – 1040 **HLS and Cost of Design**
⇓ R Gupta, UCSD, US

1045 – 1105 **Multi-Mode Architecture Design with High-Level Synthesis**
⇓ P Coussy, University of South Brittany, FR

1110 – 1130 **Ant Colony Optimization for High Level Synthesis**
⇓ R Kastner, UCSB, US

1135 – 1155 **User Guided High level synthesis**
⇓ F Pétrot, TIMA Laboratory, FR

1200 – 1300 **LUNCH**
1300 – 1430 Session 3: Posters / Demonstrations / Interactive Presentations

1430 – 1445 Break

1445 – 1645 Session 4: The Future of High-Level Synthesis

The Limits of Current HLS Offer: What is Needed for a Wider Adoption
- P Urard, STMicroelectronics, FR

"All-in-C" SoC Synthesis and Verification with CyberWorkBench
- K Wakabayashi, NEC, JP

Enabling DSP System Designs with High Level Design Methodologies & Tools
- J Heighton, Xilinx, IR

Industrial Usage of High-Level Synthesis
- W Ecker, Infineon, DE

Synthesis Semantics for SystemC
- A Takach, Chair of the OSCI Synthesis Working Group, US

Panel Discussion

- With all session 4 presenters

1645 Close