The New Wave of the High-Level Synthesis

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**Description:**

The successful usage of Hardware Description Languages like VHDL and Verilog in design flows is mainly due to the availability of efficient synthesis methods and tools that enable the translation of RTL designs into optimised gate-level implementations. Many expect that the same approach could be effectively adapted at higher levels of abstraction. In the SoCs context, the traditional IC design methodology relying on EDA tools used in a two stages design flow - a VHDL/Verilog RTL specification, followed by logical and physical synthesis - is indeed no more suitable. Thus, actual complex SoCs need new ESL level tools in order to raise the specification abstraction level up to the algorithmic / behavioural one. Languages like C/C++/SystemC offer high abstraction levels. However, in order to provide the designers with an efficient automated path to implementation, new high-level synthesis tools are required. Several commercial and academic tools are available today: Bluespec from Bluespec, Catapult from Mentor Graphics, Cyber from NEC, Synthesizer from Forte Design Systems, PICO from Synfora ... GAUT from UBS University, SPARK from UCSD, UGH from TIMA/LIP6, xPilot from UCLA...

The main expectations from the system design teams concern both methods and tools supporting better management of the design complexity and reduction of the design cycle all together, breaking the trend to compromise evaluation of various design implementation options. Designing at higher levels of abstraction is an obvious way as it allows a better coping with the system design complexity, to verify earlier in the design process and to increase code reuse.

**Target Audience:**

This workshop on High-Level Synthesis will provide an overview of existing and emerging solutions provided by both industrial partners (EDA companies) and research institutions in this domain. It will give an outline of HLS methods and tools available currently on the market and bring the details on their applicability, performance, and strengths. Finally, the event will create a discussion platform for experience exchange between providers of synthesis technology and industry users.