The 2012 System, Software, SoC and Silicon Debug Conference

Program

Vienna, Austria
September 19-20, 2012

Conference Chair:
Peter Rössler,
University of Applied Sciences,
Technikum Wien

S4D is an ecsi event!
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S4D is co-located with FDL!

S4D registration includes free access to FDL sessions on Sept. 19 & 20!
Embedded systems and software complexity is rapidly increasing; from one processor to ten or more, from thousands of lines of code to millions. Modern system-on-chips integrate dozens of hardware accelerators and I/O devices. Modern products integrate hard IP and software from many more sources than in the recent past. Embedded systems debug capabilities must scale with this exponential growth in system complexity.

This fourth edition of S4D Conference has evolved from several industry workshops organized by ECSI into the areas of debug and provides a forum for work and standardization efforts related to debug of electronic systems. The conference addresses a vast set of requirements from system and SoC companies with regard to debug methods and tools. It includes efforts from IEEE and other standards working groups, including the Nexus 5001 Forum, IJTAG (IEEE P1687), IEEE 1149.7, MIPI, industry working groups including OCP-IP, the Multicore Association (MCA), the Accellera - SPIRIT Consortium and Eclipse and industry R&D projects contributing to debug and related tools and methods development. The S4D Conference event also allows presentation and discussion of existing and new commercial debug tools and products related to electronic (silicon and software) methods, devices, and systems. In summary, the S4D Conference provides a forum for discussing research, scientific and commercial development in the areas of system, software, SoC and silicon debug.

Conference Chairs

General Chair: Peter Rössler,
University of Applied Sciences, Technikum Wien

Peter Rössler received his Diploma and Ph.D. from the Vienna University of Technology. Currently he works as a FH-Professor at the University of Applied Sciences Technikum Wien in Vienna/Austria where he is managing R&D projects in the area of embedded systems. His main research interests cover topics like FPGA, ASIC and ESL design as well as control networks (fieldbus systems). He is co-founder of a company related to building automation systems. Peter Rössler is author of 50+ publications. He is member of conference program committees like ASME/IEEE MESA, Austrochip or ME and is engaged in boards of national organizations like the Austrian Electrotechnical Association (ÖVE) or the Austrian Society of Microelectronic Systems. Since 2012 he is Chair of the IEEE Austrian Section.

Co-Chair: Adam Morawiec, ECSI

Adam Morawiec received his MSc degree in electronic system design in 1993 from the Silesian Technical University in Gliwice, Poland and his DEA (Diplome d’Etudes Approffindies) in 1996 and PhD in 2000 in Microelectronics at the TIMA Laboratory / Université Joseph Fourrier, Grenoble, France in the domain of verification and simulation performance methods. He works for in the R&D project development and management in the domain of system design methods and standards, in setting up industry and research consortia, in organization of advanced training and workshop in system design area. He also acted as an expert of the European Commission in the R&D project proposal evaluation and IST/ICT Work programmes definition. Since 2005 he is the director of ECSI. He is an author of several scientific publications in the area of formal verification, formal models, simulation performance and system design. He is also an editor of two technical books published by Springer Publishers: “Platform Based Design at the Electronic System Level" and "High-Level Synthesis".
Keynote Speakers

Albrecht Mayer, Infineon
Albrecht Mayer is Senior Principal Emulation Systems and Tooling at Infineon. Within the automotive microcontroller business unit he is responsible for on-chip debug architectures and C-modeling methodology. He defined with his team the TriCore™ debug architecture, which is the benchmark in the automotive industry. He has published many papers and holds more than 20 patents. Dr. Mayer received Diploma and PhD degrees in electrical engineering from the Technical University of Munich.

Ingo Sander, KTH Royal Institute of Technology
Ingo Sander received the MSc degree in Electrical Engineering from the Technical University of Braunschweig, Germany, in 1990 and the PhD degree from KTH - Royal Institute of Technology, Sweden, in 2003. Between 1991 and 1993 he has worked as system design engineer at Ericsson, Sweden. In 1993 he joined KTH, where he since 2005 holds a position as associate professor in Electronic System Design. His main research interests are located in the area of design methodologies for embedded systems. His current research is aiming towards predictable performance of real-time applications on multi-processor platforms by integration of formal models into the design flow.

Program Committee

Tapani Ahonen
Jens Braunes
Pat Brouillette
Philippe Cuenot
Serge De Paoli
Jakob Engblom
Philipp Graf
Jan Haase
Ziyad Hanna
Andreas Hoffmann
Rolf Kühnis
Rainer Leupers
Andrea Martin
Albrecht Mayer
Tampere U. of Technology
PLS Development Tools
Roku
Continental Automotive
STMicroelectronics
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Synopsys
Intel
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Adam Morawiec
Brenden Mullane
Chris Ng
Frédéric Petrot
Paolo Prinetto
David Riemens
Neal Stollon
Erich Styger
Bart Vermeulens
Alexander Weiss
Michael Williams
Markus Winterholer
Hans-Joachim Wunderlich
U. of Essex/UltraSoC
ECSI
U. of Limerick
IBM
TIMA Laboratory
Politecnico di Torino
NXP
HDL Dynamics
Freescale
NXP
Accemic
ARM
Cadence
U. of Stuttgart
LieberLieber AMUSE is a simulation tool for UML or SysML and a model debugger. The product is the result of our rich experience gained in various system engineering projects over the last years. We strongly believe that the model-based software and system engineering will determine the future of the industry sector and we are proud to support the trend with our products.
Multi-core is on the way becoming standard also in automotive and industrial hard real time systems. For reducing complexity the software design is top-down with abstract, e.g. graphical, control algorithm design and code generation. This flow works well and in theory it’s correct by construction but in practice there are always cases which needed to be analyzed in detail. This leads to the requirement of using and connecting different tools in parallel. However since this is done just during the development phase there is always the pressure to use as few as possible package pins for that. This talk will summarize requirements and show solution examples from Infineon’s AURIX automotive microcontroller family, but point out also still existing gaps and future needs.
Wednesday, September 19, 2012
13:30-14:30

Session 1: Software Instrumentation

*Minimising the Impact of Software Instrumentation Using On-chip Debug and a Secondary CPU Core*
Padraig Fogarty (University of Limerick)

*Software Instrumentation of Safety Critical Embedded Systems - a Problem Statement*
Mathias Ekman and Henrik Thane (Mälardalen University)

Coffee Break
14:30-15:00

Wednesday, September 19, 2012
15:00-17:00

Session 2: Profiling, Runtime Verification, Reverse Debug and Speedpath Diagnosis

*Profiling Bare-Metal Cores in AMP Systems*
Adriaan Schmidt (Fraunhofer ESK)

*A Runtime Verification Unit for Microcontrollers*
Thomas Reinbacher, Andreas Steininger (Vienna University of Technology), and Martin Horauer (University of Applied Sciences Technikum Wien)

*A Review of Reverse Debugging*
Jakob Engblom (Wind River)

*Application of Timing Variation Modeling to Speedpath Diagnosis*
Mehdi Dehbashi and Görschwin Fey (University of Bremen)

Social Event 17:00-21:00

*Please meet at the registration table at 17:00 for departure.*
Advances in process technology have led to extremely powerful many-core platforms, but in practice it is very difficult to exploit their inherent potential. Instead, in particular in the real-time domain, the verification costs often dominate the design costs due to a lack of design methodologies capable of handling the increasing complexity of large heterogeneous and inherently parallel embedded systems. Simulation is still the dominating verification technique in industry and can only indicate, but not prove the correctness of an implementation. In recent years, research has significantly improved the possibility for a correct-by-construction design flow, especially in areas like predictable architectures and models of computation. The keynote discusses the current situation, analyzes prerequisites and provides suggestions towards a correct-by-construction design flow, which could drastically reduce the verification costs.

Coffee Break 10:30-11:00

Thursday, September 20, 2012
11:00-12:30

Session 3: Verification and Virtual Prototyping

Co-Debug and Co-Verification Environment for Power Management System
Markus Winterholer (Cadence)

Scalable and Retargetable Debugger Architecture for Heterogeneous MPSoCs
Luis Gabriel Murillo, Julian Harnath, Rainer Leupers and Gerd Ascheid (RWTH Aachen)

Co-Simulation Framework for Variation Analysis of Radio Frequency Transceivers
Sumit Adhikari, Florian Schupfer and Christoph Grimm (Vienna University of Technology)

Lunch 12:30-14:00

Thursday, September 20, 2012
14:00-15:30

Session 4: Tracing

Compact Function Trace (CFT)
Albrecht Mayer and Reinhard Deml (Infineon)

CULT: A Unified Framework for Tracing and Logging C-based Designs
Wei Hong, Alexander Viehl (Forschungszentrum Informatik Karlsruhe), Nico Bannow, Christian Kerstan, Hendrik Post (Robert Bosch GmbH), Oliver Bringmann and Wolfgang Rosenstiel (University of Tuebingen)

ARMv8 Debug and Trace Architectures
Michael Williams, ARM Limited
Welcome to Vienna

Welcome to Vienna, the largest and most populous city in Austria as well as a cultural, economic, and political centre.

The 15th annual FDL Conference is held at the Vienna University of Technology, situated in the heart of Vienna. Within walking distance are the Opera House, the art nouveau Secession building, the Musikverein, home of the Vienna Philharmonic, from where the New Year’s Concert is annually broadcast around the globe, and the splendid baroque Karlskirche (Church of St. Charles).

Vienna University of Technology
Gusshausstr. 27-29, 1040 Wien
Building C, part CA
(main entrance of C)

Language

The language of the conference will be in English.

Rooms

FDL: EI9 & EI10
Event B Tutorial: CDO404
FDL PC Meeting: CDO404
S4D: EI8
ESCUG Meeting: EI10

Conference Hours

Conference/Registration Hours:
- Wednesday 8:00 – 17:00
- Thursday 8:30 – 15:30

Social Event

The 2012 FDL Social Event will start with an exclusive tram ride around the Ringstrasse, a circular road surrounding the Innere Stadt district of Vienna, Austria and one of its main sights. Following the historic tram ride, the participants will be led through a guided tour at the Albertina, one of the most famous museums in the world. The Social Event will then conclude with dinner at the Augustinerkeller restaurant near the Albertina.

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