Successful system integration will rely on the use of applicable and efficient standards by the different partners involved in the system design process. An industry-wide synergy in the development, evaluation and adoption of these standards is required. They will boost the capabilities of specification, verification and implementation methods combined and contribute to decrease the productivity gap of the design process of complex embedded systems. This workshop is organised to update ECSI members or guests with the information about the emergence and evolution of some of the most important standards in system design domain: in system specification (UML, PSL), and in system design and implementation (SystemVerilog, SystemC, VHDL 200X, SystemC-AMS extension, OCP-IP standards).

The workshop sessions will encompass the current status of the standardisation process, future plans for standard evolution as well as technical introduction and overview of the standards. It will also bring an industry point of view on the requirements for standards in system design. The objective of this event is to present system level standardisation activities by ECSI members to other ECSI members. The information specifically related to standardisation process is presented under control of the appropriate standardisation bodies or working groups chairs.

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**Agenda**

9:00-9:15 Welcome

9:15-10:15 The **Unified Modeling Language**: UML v2.0 and specialised profiles
- Standard evolution at OMG - *Francois Terrier, CEA*
- Technical presentation – *Marko Boger, CEO, Gentleware*

10:15-10:30 The **Accellera standards**: PSL and SystemVerilog
- Accellera standardisation update - *Dennis Brophy, Mentor Graphics - Accellera Chairman*

10:30-10:45 Break

10:45-12:00 **Property Specification Language**: PSL
- PSL Syntax, PSL Tools, Discussion, IBM Perspective - *Yaron Wolfsthal, IBM*

12:00-12:45 System extensions to HDLs: SystemVerilog
- Technical update - *Peter Flake, Synopsys*

12:45-13:45 Lunch

13:45-14:20 The **OSCI standard**: SystemC
- SystemC standardisation activities – *Alain Clouard, ST Microelectronics*
- Technical update on SystemC (2.0.1) *Axel Braun, ESCUG / University of Tübingen*

14:20-15:00 **SystemC/SystemVerilog relation**
*Markus Wloka, Director R&D, Synopsys Verification Group*

15:00-15:45 System extensions to HDLs: IEEE/VHDL 200X
*Gabriel Chidolue, Mentor Graphics UK*

15:45-16:00 Break

16:00-17:00 Open Core Protocol International Partnership
*Ian Mackintosh, Sonics, Inc. – OCP IP President*

17:00-17:25 System company requirements for industry standards in system design
*Christophe Gendarme, Alcatel*

17:25-17:45 Emerging candidate standard: SystemC-AMS
*Alain Vachoux, EPFL*

17:45-18:00 Discussion and workshop wrap-up